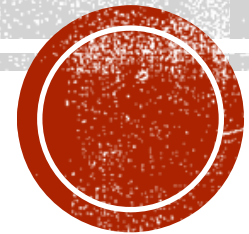


INTRODUCTION TO VHDL



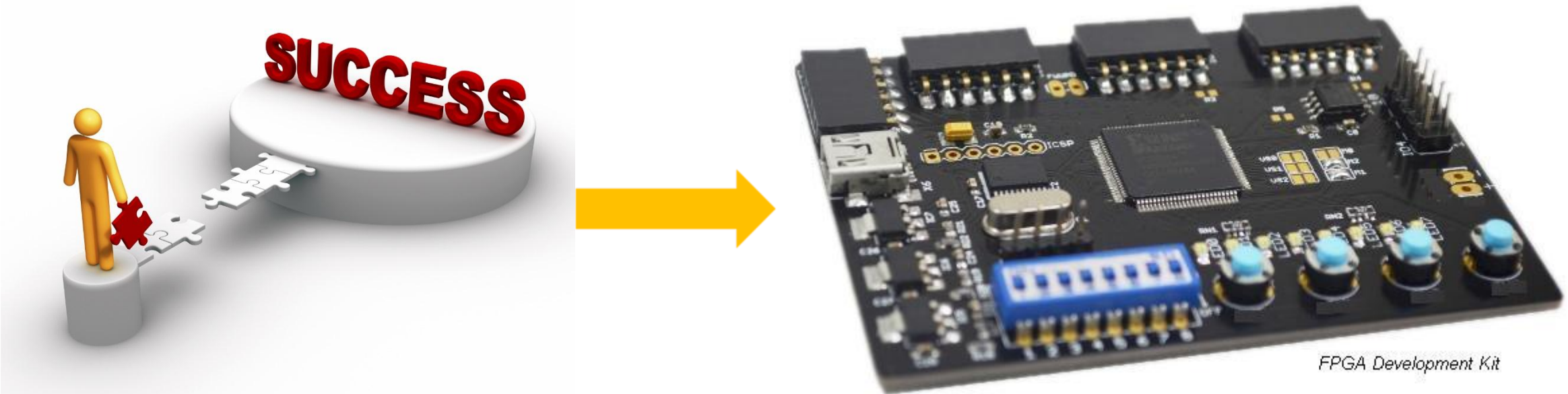
Ali Kanaan

VHDL !! WHAT IS THAT !!

- Describe your hardware !
- Test it and get waveforms !
- Combine it with other components (y)
- Synthesize it :P
- Implement it by injecting the synthesized into chip ☺
- ** develop and build your ideas (y)



PROJECT CONSTRUCTION



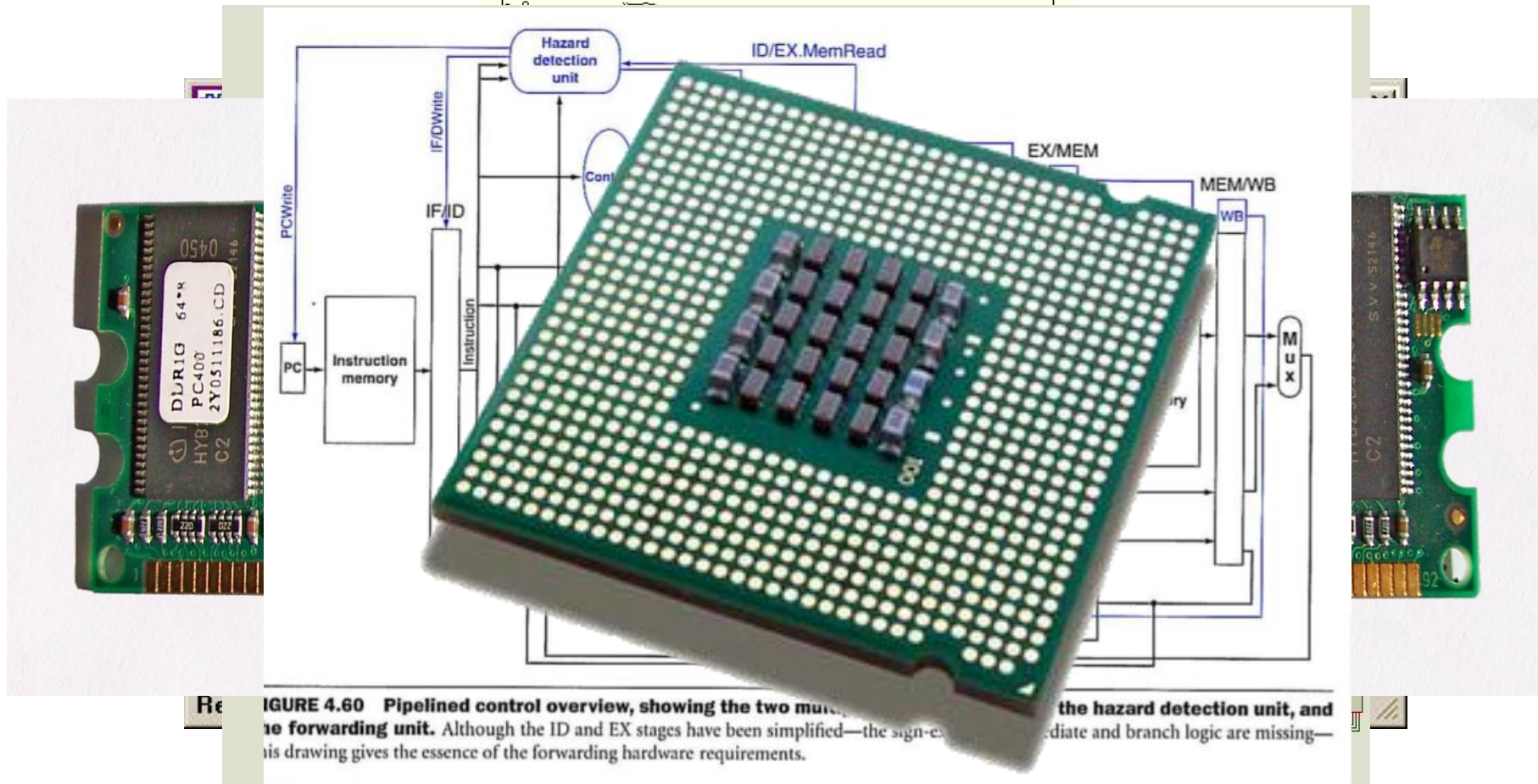
WHAT YOU SHOULD KNOW

- Simply, before start using VHDL you should know the domain you work on or have a full view on the project you work with
ie. Logic design, PID, machine learning etc..
- Be familiar with programming language.. There is more than a language to learn here ;)
- Get used to work in a team.. VHDL was developed mostly for that reason 😊

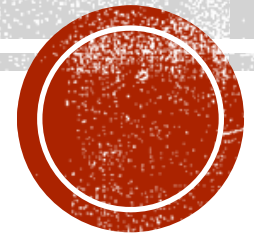




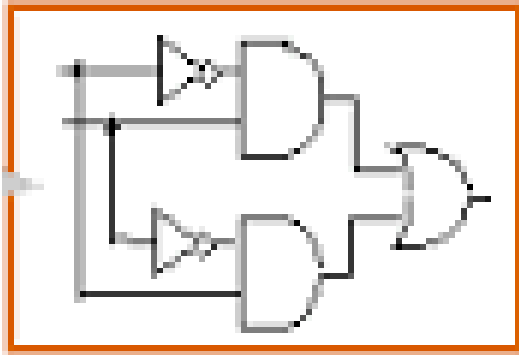
CAPABILITIES



BEHAVIORAL AND STRUCTURAL

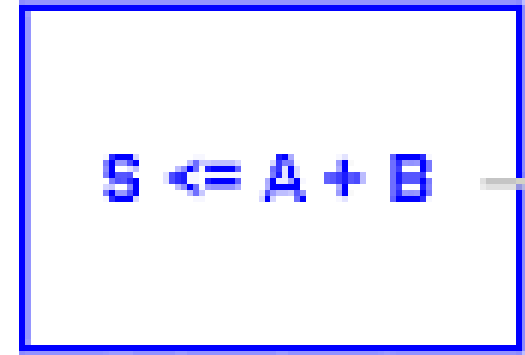


IDEA

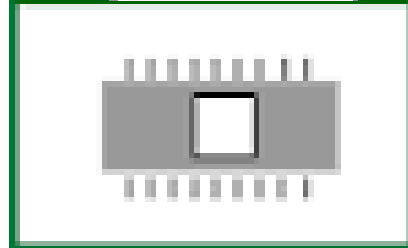


Structural
(components-
interconnections)

But I need components that
Can I just write its behavior ???
I can't build its structure



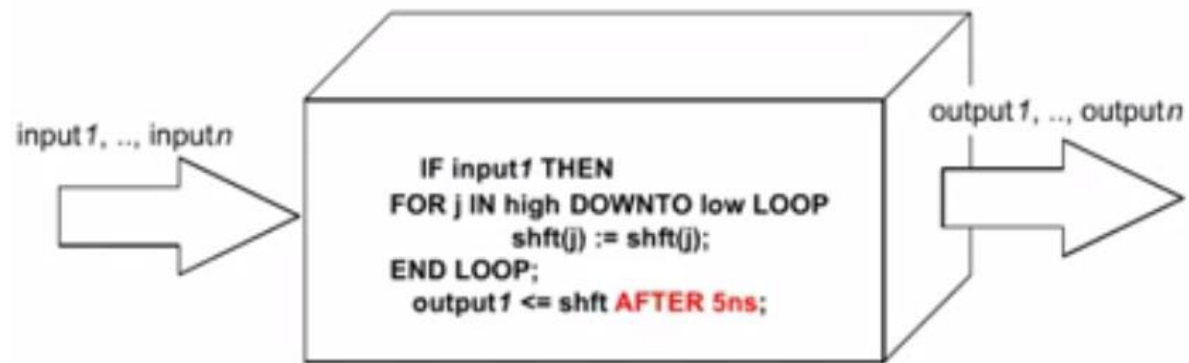
Behavioral
* Algorithmic
* Dataflow



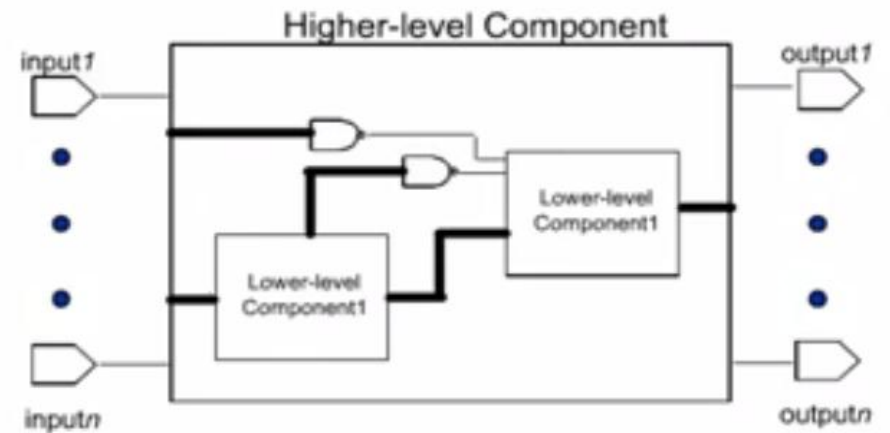
Physical
(implementation)



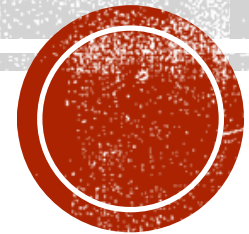
Behavior



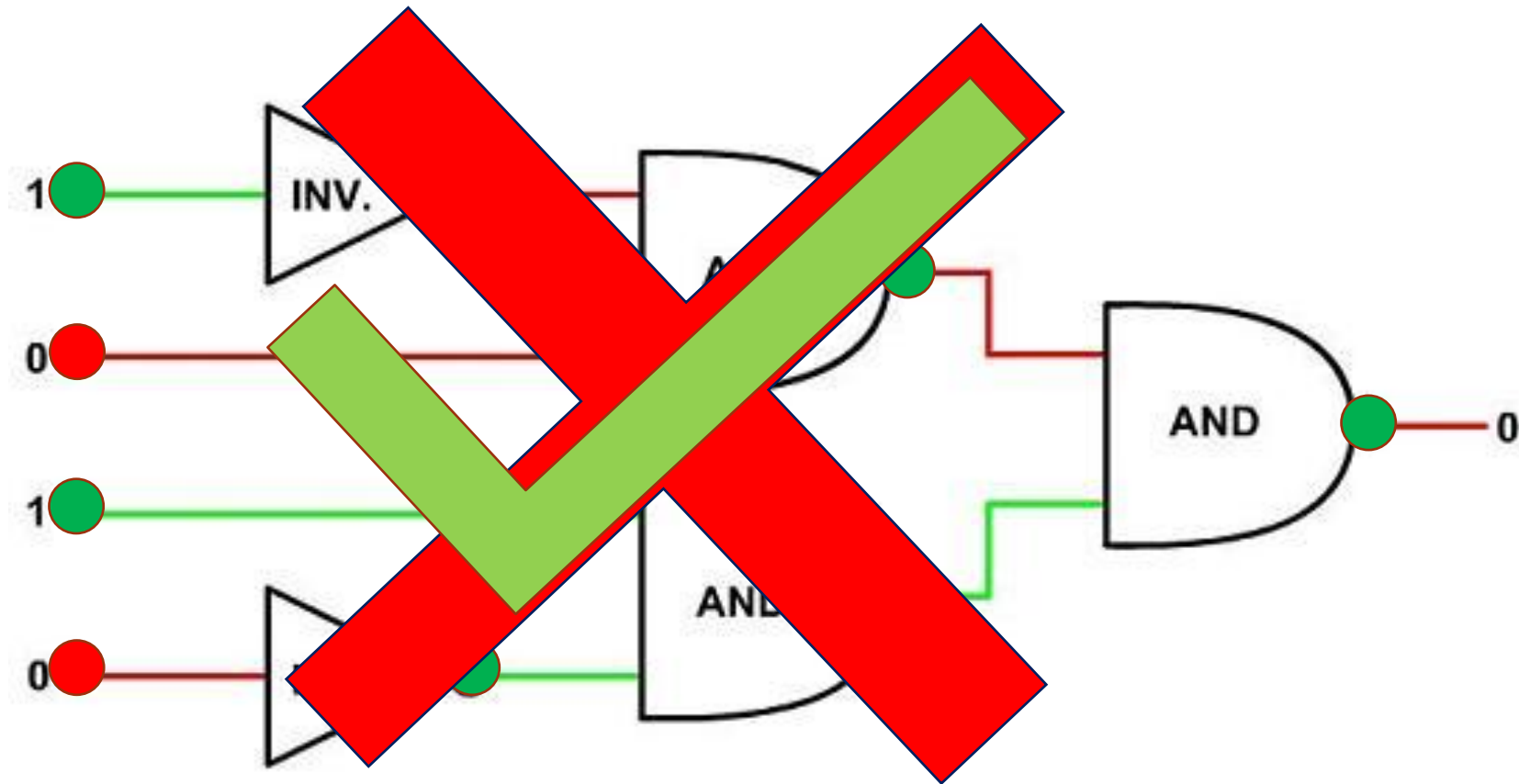
Structure



PARALLEL EXECUTION

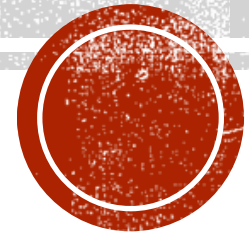


NATURE



SYNTHESIS AND SIMULATION

Introduction



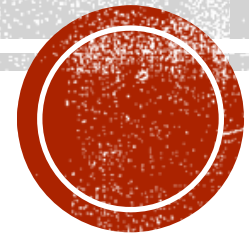
WHEN REQUIRED

- يتم استخدام لغة VHDL من اجل محاكاة نماذج صلبة ولكن لا يمكن انشاء كل ما يتم محاكاته
- بعض تعليمات VHDL تستخدم لمحاكاة تصرف البنية ولا يمكن ان تتحول لبنية صلبة تنتج نفس نتائج المحاكاة ويسمى ملف ال VHDL الذي لا يتميز بقابلية تحويله الى بنية حقيقية يتم حقنها بملف غير تركيبى والعكس بالعكس
- مثال عن تعليمات غير قابلة للتركيب :
 - الحلقات
 - System calls
 - Wait and sleep statement
- تتم محاكاة ملف ال VHDL ضمن بيئة Active HDL عن طريق تشكيل موجات منطقيه من تتالي ٠ منطقي و ١ منطقي على الدخل ومراقبة الخرج عند كل حالة دخل.



APPLICATIONS

Introduction





RELATIONS

Hardware design
Digital design

